Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A configurable interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via a first external signal path;

a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;

an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and

a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal.

2. (Canceled)

3. (Original) The configurable interface circuit of Claim 1, wherein:

the first internal signal path and the first external signal path are operable to propagate signals in accordance with a common protocol.

4. (Original) The configurable interface circuit of Claim 3, wherein:

protocol is a PCI bus protocol.

5. (Original) The configurable interface circuit of Claim 3, wherein:

protocol is an AGP bus protocol.

6. (Original) The configurable interface circuit of Claim 3, wherein:

protocol is an NGP bus protocol.

7. (Canceled)

8. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the second internal circuit is operable to provide the second internal signal via the second internal signal path to both the first internal circuit and the output buffer.

9. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the second internal circuit is operable to receive a selected signal that is either the first internal signal or the first external signal from the selector circuit, and inoperable to receive the second internal signal from the selector circuit.

10. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the second internal circuit is operable to provide the second internal signal to the first internal circuit via a fourth internal signal path when the second internal circuit is in a first mode, and to provide the second internal signal to the output buffer via the second internal signal path when the second internal circuit is in a second mode.

11. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the second internal circuit comprises a bus interface.

12. (Original) The configurable interface circuit of Claim 11, wherein:

the second internal circuit is a bus bridge.

13. (Original) The configurable interface circuit of Claim 1, wherein:

the first internal circuit comprises a bus interface.

14. (Original) The configurable interface circuit of Claim 11, wherein:

the first internal circuit is a graphics controller.

15. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the first internal circuit is operable to receive the second internal signal via the second internal signal path.

16. (Previously presented) The configurable interface circuit of Claim 1, further comprising:

a bus bridge, comprising a bus interface, operable to provide a second internal signal to the first internal circuit via a second internal signal path and to receive the selected signal via a third internal signal path.

17. (Original) The configurable interface circuit of Claim 16, wherein:

the first internal signal path and the first external signal path are operable to propagate signals in accordance with a common protocol.

18. (Original) The configurable bus interface circuit of Claim 1, wherein:

the selector circuit is operable to provide a selected signal that is uncorrupted by transmission line effects.

19. (Original) The configurable bus interface circuit of Claim 1, wherein:

the input buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

20. (Previously presented) The configurable bus interface circuit of Claim 1, wherein:

the input buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit; and

the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

21. – 39. (Canceled)

40. (Previously presented) A configurable interface circuit comprising:

an internal graphics controller operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via a first external signal path;

a selector circuit coupled to the internal graphics controller via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;

a bus bridge, comprising a bus interface, operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and

an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

41. – 43. (Canceled)

44. (Previously presented) A configurable bus interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer, operatively coupled to a first external signal path, and to the first internal circuit via the first internal signal path, and operative to receive the first internal signal from the first internal signal path and to provide the first external signal on the first external signal path;

a selector circuit, operatively coupled to the first internal circuit via the first internal signal path, and to the input buffer, and operative to cause the input buffer to provide the first internal signal from the first internal signal path to the first external signal path, and to isolate the first internal signal on the first internal signal path from the first external signal;

an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and

a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal.

45. (Previously presented) The configurable bus interface circuit of claim 44 including:

a first external circuit, operatively coupled to the input buffer via the first external signal path to receive the first external signal, such that the input buffer is operative to provide the first internal signal from the first internal signal path to the first external signal path, and to prevent the first internal signal on the first internal signal path from propagating to the first external signal path.